Next Generation Ultra Thin HDI PCB Manufacturing Challenges for Airborne Radar Applications

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***Abstract*—** In recent years, with the development trends towards lighter and smaller high performance and high reliability electronic products, printed circuit boards have ceaselessly been growing in terms of higher density and layer count. High-density interconnection (HDI) PCB technology is advancing to enable increased miniaturization and functionality of products & this dictates continual reduction in feature size for conductor line width and spacing, micro-via pad diameter and pitch, and conductor and insulating layer thickness to accommodate more components and layers without increasing size, weight or volume of the PCB assembly. Fortunately, laminate manufacturers have responded to these challenges by developing and introducing a wide range of new laminates that address these issues. This paper will describe the recent challenges and developments in manufacturing HDI technology to meet the needs for high volume, robust, reliable, and cost competitive solutions for electronic packaging.

***Keywords*— High density Interconnect(HDI) PCBs , Materials for HDI PCBs , Manufacturing techniques of HDI PCBs**

I. INTRODUCTION

Air borne radar systems realized with phased array antennas offer several advantages over systems using a conventional parabolic dish or mechanically steered antenna. A phased array antenna comprising several radiators or elements, coherently combined to form a directive antenna beam that can be steered electronically by applying linear phase progression between the elements became extremely advantageous for modern radar applications, which usually require very high gain antennas. Performance, flexibility and reliability are some of the advantages of an electronically scanned radar antenna as compared to its mechanically scanned counterparts. After many years of development the active electronically scanned array radar technology has reached a matured technology level. Many of the today's and future radar systems will be equipped with this technology. The electronic systems used for these radar systems function largely on complex, highly reliable electronic circuitry.

Moreover with the rapid expansion of the internet, the enhancement of information systems is common goal of the developers of electronics, information and communication equipment. Personal computers and cellular phones in consumer electronics are competing for small form factors, light weight and added functions and based on this electronic devices, optical communication equipment and computer peripherals are undergoing major change in defence sector w.r.t functional enhancement. System in Package (SiP) and System on Package (SoC) gave a complete solution for replacing bare chips on a substrate in a single package. These changes in packaging technology created a big impact on, and fast evolving changes in, printed circuit boards. A method of attaching bare semiconductor chips onto a printed circuit board is emerging as high density packaging solution. The continuing increase in component performance and lead density, along with the reduction in package sizes have required that Printed circuit board (PCB) technology find corresponding ways to increase the interconnection density of the substrate. In order to support future needs, PCBs are expected to accommodate high I/O fine-pitch devices as well as small foot-print area-array packages such as chip-size packages(CSP), flip-chip attach(FCA) and direct-chip attach(DCA). Providing high-density interconnection (HDI) with blind/buried vias is a technology that holds promise in reducing layer count and board size for greater packaging efficiency. For about a decade, the technology has drawn heavy attention of PCB manufacturers worldwide. HDI is a large and growing PCB application market. The present paper describes different manufacturing techniques involved in realizing High Density Interconnects(HDI) PCBs for high reliability electronic circuitry[1].

II. IMPACT OF ULTRA FINE PITCH PACKAGES

The most common practice of increasing interconnection density of PCB is to increase the number of metal layers and control the total thickness of both dielectric material and metallization. The use of more complex components with very high I/O counts has pushed board fabricators to examine techniques for creating smaller vias. The present generation of HDI printed circuit boards are characterized by blind, buried and through vias made by techniques other than mechanical drilling. In order to turn

blind vias into buried vias, these process techniques are repeated and the layers are built sequentially. These processes adopt different methods of creating vias, such as laser drilling, additively creating dielectric with via holes using photo sensitive dielectric material and new methods of metalizing the vias such as conductive adhesives and solid paste vias [2]. At present, the design rule used for realizing HDI PCBs is summarized in Table 1.

TABLE 1

Item	Current	Future
Line width µm	100 to 50	50 to 10
Line spacing µm	100 to 60	50 to 15
Conductor thickness µm	20 to 15	15 to 10
Via diameter µm	150 to 80	80 to 40
Pad diameter µm	400 to 200	200 to 800
Dielectric thickness µm	80 to 40	30 to 20
Total board thickness µm	1000 to 500	800 to 300
Layer count	6 to 16 layers	6 to 20+ layers

III. SEQUENTIAL BUILD-UP

A recent major change in manufacturing printed circuit boards is the rapid popularization of Sequential Build-Up (SBU) processes[1]. The SBU process, although first published in 1976, attracted the attention of printed circuit board industry only in 1991, when IBM Japan announced the implementation of this technology. A number of product development reports started to appear around 1996, and volume productions started in Japan around 2002. When performance improvements are required for PCBs, HDI is the leading contributor. In addition to making PCBs smaller, lighter & thinner, HDI will give them superior electrical performance. With layer counts increasing & drilled hole sizes decreasing, it seems logical to explore ways to increase interconnect density, decrease layer thickness & incorporate smaller vias whereever possible. These factors culminated in the introduction of microvia technology for HDI or Sequential build-up (SBU) of multilayers in the PCB industry

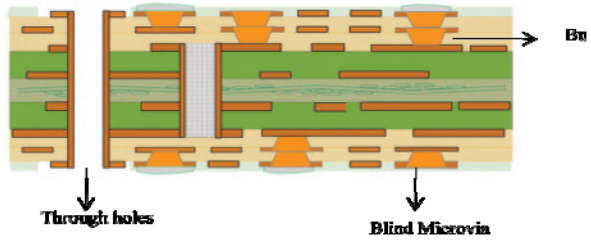

FIGURE 1:
Cross section of HDI board with microvia

III. HDI PCB CONSTRUCTION

The four common approaches followed for HDI PCB stackups as defined by Institute for Interconnecting and Packaging Electronic Circuits (IPC) are as follows:

i. *Through Vias from Surface to Surface*
ii. *Staggered & Stacked Sequential Microvia Build-up*
iii. *Co-Laminated Any layer Microvia Build-up*

These stack-ups are followed based on the complexity of the system & the user requirement.

Through Vias from Surface to Surface

In this construction both plated microvias and plated through holes are used for interconnections. The printed circuit core is typically manufactured using conventional printed circuit techniques. A single layer of dielectric material is then placed on top of the core substrate. Microvias are formed in the dielectric connecting layer 1 to layer 2 and layer n to layer n-1. Through- holes are then drilled connecting layer 1 to layer n. The microvias and through-holes are then metalized or filled with conductive material. Layer 1 and layer n are circuitized and fabrication is completed. Figure 2 shows the 6 layered multilayer stackup of an HDI PCB composed for multilayers drilled and plated & then laminated to rigid core.

FIGURE 2
Through Vias from Surface to Surface

Staggered & Stacked Sequential Microvia Build-up

In this construction the of two microvias layers are fabricated on either side or both sides. [1]It also allows through vias to be placed in the core before HDI layers applied. The printed circuit core is typically manufactured using conventional printed circuit techniques. A single layer of dielectric material is then placed on top of the core substrate. Microvias are formed in the dielectric connecting layer 2 and layer 3 and layer n-1 and layer n-2. This first microvia layer is either metalized or filled with conductive materials and then circuitized. A second layer of dielectric material is then placed on top of this circuitized layer and microvias are formed connecting layer 1 to layer 2 and layer n to layer n-1. Though holes are then drilled connecting layer 1 to layer n. The microvias and through-holes are then metalized or filled with conductive material. Layer 1 and layer n are circuitized and fabrication is completed. Figure 4 shows the 8 layer staggered

multilayer stack up with one build-up layer on each side of an eight layer multilayer board, mechanical / laser drilled and plated and then laminated. Figure 3 & 4 shows the eight layer stacked multilayer board, laser drilled and plated and then laminated twice.

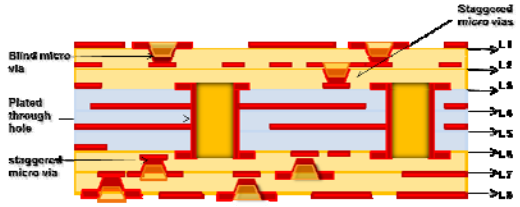

FIGURE 3
Staggered Sequential Microvia Build-up

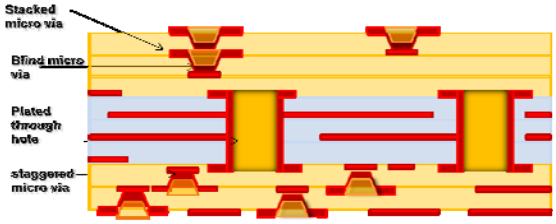

FIGURE 4
Stacked Sequential Microvia Build-up

Co-Laminated Any layer Microvia Build-up

In this construction there is no core. Both plated & conductive paste layer pairs are interconnected through a co-lamination process. Layer pairs are prepared using the conventional processes of etching, plating and drilling etc., or by conductive paste processes. The layer pairs are then laminated together. Figure 5 shows the eight layer multilayer stackup composed of four double-sided layer pair cores. Each mechanically or laser drilled and plated and then laminated

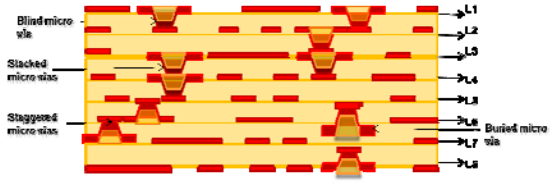

FIGURE 5
Co-laminated any layer Microvia build-up

IV. MANUFACTURING CHALLENGES

Microvia formation

An SBU process is highly effective in reducing via diameters and in expanding the space available for routing conductor lines. The capability of making high-density fine-line circuitry in the newly acquired space depends on the manufacturing processes such as drilling methods, plating methods and imaging processes. Therefore, the most important goal is the establishment of a process technology for miniaturization of the circuitry on each layer.

Analysis for different mechanical and laser techniques for microvia formation shows that mechanical drilling is a proven technology that covers a large range of via diameters with high aspect ratios (ratio of depth to width). The use and popularity of blind & buried vias has accelerated the trend to explore special techniques to achieve depth controlled drilling for smaller via sizes (microvias). High speed spindles combined with Electric Field Sensing (EFS) technique can be used for the drilling microvias with mechanical drilling machines. With these improvements and good quality of tungsten carbide drill bits, there is greater opportunity to start manufacturing microvias with CNC drilling machines for HDI PCBs.

Laser drilling is the present and latest trend of microvia generation techniques. Laser via processing is by far the most popular for high volume production of blind vias and microvias world wide. The laser is the most common method of production of microvias to be plated or filled with a conductive paste. Most laser processes utilize either carbon-di-oxide or UV lasers. Carbon dioxide combination lasers are the most popular at present. The selection of a thinner foil, utilization of half-etch technique (etch-down to half of the original thickness), or fully etched copper foil (utilization of surface roughness created by the copper foil) are challenges of the process. Recent developments allowed direct laser drilling though a copper foil with a carbon dioxide laser / Nd:YAG thus eliminating the need of a conformal mask. In HDI process it is important to optimize the laser drilling conditions for the via formation.

[3]The interconnections between multiple layers of conductors by via connections in SBU printed circuit boards are normally implemented by staggered vias, as shown in Figure 7 (a). Microvias filled with conductive material have sufficient physical strength and electrical conductivity. Stacked vias shown in Figure 7 (b), filled with a plated post, are often referred to as “filled vias.” Periodical Reverse (PR) current plating and pulse plating were found to be effective and the complete filling of vias was accomplished by the adjustment of plating additives with direct current. In a production environment, extensive technique is required to control the uniformity of the plating thickness on the panel surface, as well as in the holes. Stack via process – makes via posts and surface conductors by a pattern plating or semi-

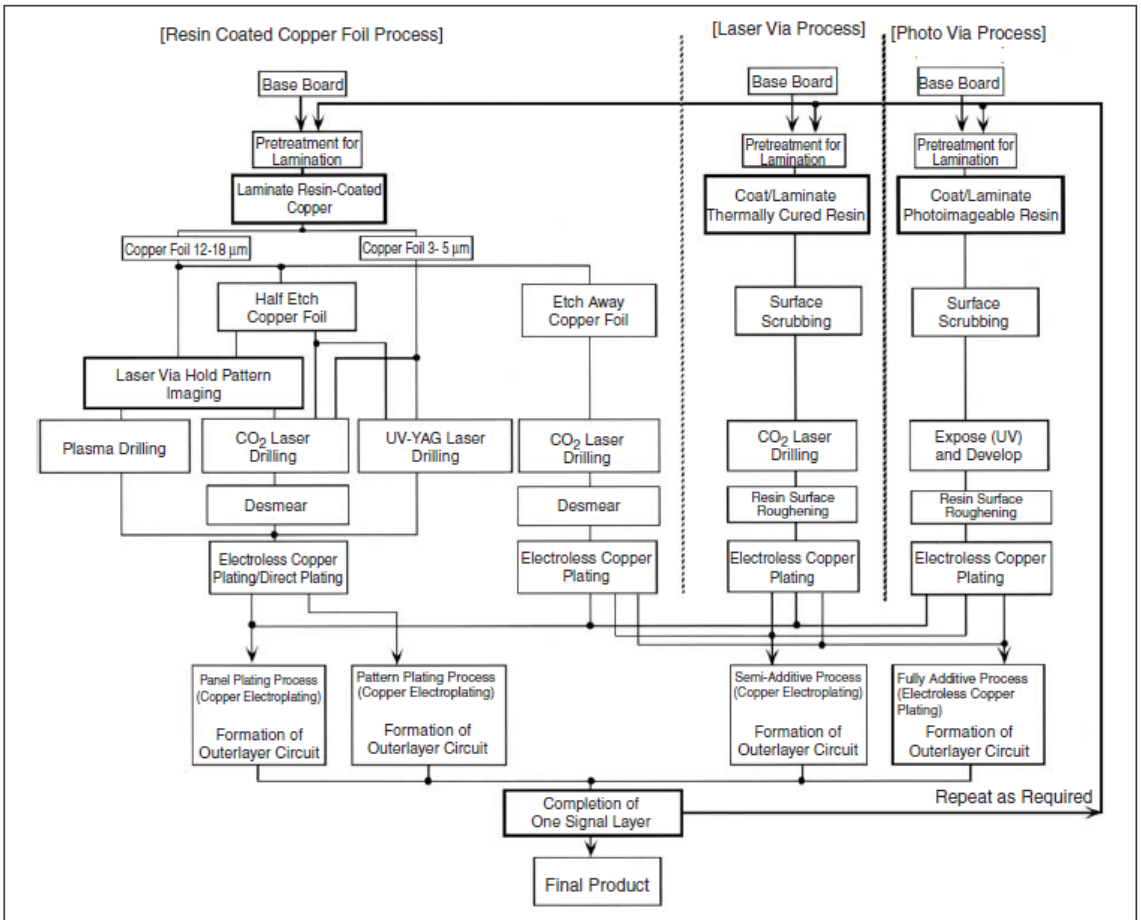

FIGURE-6: SBU Processes

additive process& multiple layer connection is achieved by conductive paste filling.

FIGURE 7(a) ***Staggered Microvia***

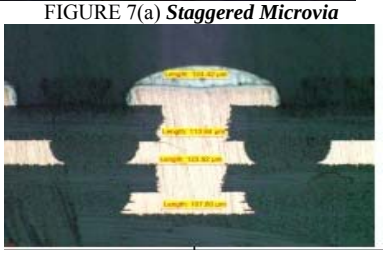

FIGURE 7(b) ***Stacked Microvia***

Plating process and Imaging of Circuit pattern

Metallization is a critical process for a reliable plated through hole, blind/buried vias and microvias. The process of making the via conductive determines whether or not the subsequent electrodeposited copper is continuous and adherent to the resin. The SBU processes with plated vias are similar to the plated through hole process of conventional multilayer printed circuit boards. By comparison, the SBU process has areas of different materials, where a resin-coated copper foil, thermally cured resin and photoimageable resin are used, and in drilling, where laser drilling or photolithography is used instead of mechanical drilling..

There are four types of SBU process, depending on the plating methods

Subtractive process (with copper foil)
_ panel plating process
_ pattern plating process
Additive process (without copper foil)
_ semi-additive process
_ fully additive process

A subtractive process starts with drilling and is followed by electroless copper plating. After the copper electroplating step, the processes are different for the panel plating process and the pattern plating process, shown as in Figure 6. In the panel plating process, electroplating covers the whole surface of a panel, etching resist is applied, and then etching is carried out to leave the circuitry. In the pattern plating process, the electroless copper surface is covered by plating resist to make openings in area where the plating should be conducted, copper electroplating is carried out in the circuit area, a metal, which has etching resistance, is further plated and a circuit pattern is created by resist stripping, etching and resist metal stripping.

Pattern plating process gives better accuracy in the circuit reproduction and panel plating process is used for imaging of the circuit pattern in the resin-coated copper foil process. The panel plating process, has an advantage in the uniformity of plating thickness over the whole surface of the panel.

An additive process is defined as a manufacturing process with no copper foils involved. In a semi-additive process and a fully additive process the circuit is created only by electroless plating. The plating resist in this process stays as

a soldermask on the board and high level of technology is required, including the plating bath control systems, to maintain the copper electroless plating solution to ensure the ability to deposit plating layers. The adhesion of the plated conductors in sequential build up layers, an important requirement of this process, is being improved because of the technological progress in roughening resin surfaces. A semi-additive process, a variant of the pattern plating process. The semi-additive process, similar to the pattern plating process, produces conductors with a small width and a large thickness. The introduction of a semi-additive process is easy when photoimageable dielectric resin or thermally cured dielectric resin is used. The pattern electroplating of copper is carried out over an electroless copper plating of 2 to 3 µm thickness. This is a process most suited for fine-line circuitry, although measures must be taken to get a uniform thickness of copper electroplating.

Metallization with electroless copper for microvias for high aspect ratio microvias is the most acceptable technology. Pulse plating techniques are being used for metallization of the via with electrodeposited copper.

V. SUMMARY

A closer look at key HDI manufacturing processes and their impact on cost and technology benefits has to be taken in account when selecting the optimized process, and therefore, a major opportunity to meet the current and future needs of electronics packaging must be considered. The functionality increase and size reduction are not the only challenges for HDI PCBs. The increasing operating frequencies with ultrathin constructions will play a more important role in near future end products. Subtractive process ultimately faces limitations of nominal thickness and thickness variation and is sensitive to conductor spacing and base foil roughness. Additive processes have fundamentally higher system resolution and superior conductor geometry but are complex to engineer / control. There is no easy answer for manufacturing process selection as it depends on the product design features. Early involvement in design process is helpful for finding the most cost effective solution.

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